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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/363,311
Filing Date: July 28, 1999
Appellant(s): WATKINS, DANIEL

Daniel Watkins
For Appellant

EXAMINER'S ANSWER

1. This is in response to the appeal brief filed 20 August 2003.

Real Party in Interest

2. A statement identifying the real party in interest is contained in the brief.

Related Appeals and Interferences

3. A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

Status of Claims

4. The statement of the status of the claims contained in the brief is correct.

Status of Amendments After Final

5. The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

Summary of Invention

6. The summary of invention contained in the brief is correct.

Issues

7. The appellant's statement of the issues in the brief is correct.

Grouping of Claims

8. Appellant's brief includes a statement that claims 1-20 stand together.

Claims Appealed

9. The copy of the appealed claims contained in the Appendix to the brief is correct.

Prior Art of Record

5,949,691	KUROSAKA et al.	9-1999
6,141,630	MCNAMARA et al.	10-2000
5,684,808	VALIND	11-1997

Grounds of Rejection

10. The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6, 8, 9, 11-14 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosaka et al. (U.S. Patent No. 5,949,691) (hereinafter Kurosaka, in view of McNamara et al. (U.S. Patent No. 6,141,630) (hereinafter McNamara).

Referring to claim 1, Kurosaka discloses a system for device verification (see Kurosaka., Figure 1, i.e. logic circuit verification device 100) comprising; a profile generation module (see Kurosaka, Figure 1, i.e. data input unit 101) configured to provide a pattern profile (see Kurosaka, Figure 1, i.e. intermediate format data file 106) that represents a test pattern, wherein the aspects are specified by a profile mode (see Kurosaka, column 8 lines 34-40), a coverage measurement module (see Kurosaka,

Figure 1, i.e. corresponding point detection section 102) configured to process the pattern profile (see Kurosaka, Figure 1, i.e. intermediate format data file 106) to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module (see Kurosaka, Figure 1, i.e. data input unit 101) is further configured to process the analysis results to provide an improved pattern profile (see Kurosaka, column 9 lines 31-40), and a pattern generation module (see Kurosaka, Figure 1, i.e. corresponding point detection section 102) configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance (see Kurosaka, column 8 lines 41-49). Kurosaka does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara teaches a test pattern as a time sequence (see McNamara, column 4 lines 46-65) of input signal vectors (see McNamara, column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara, column 5 lines 49-54 and column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara, column 6 lines 8-19).

Referring to claim 2, Kurosaka further discloses a coverage measurement module which is configured to determine coverage of the test pattern by ascertaining if

node faults are detectable, wherein node faults are detectable if running the test pattern on a device would indicate a failure (see Kurosaka, column 11 lines 47-55 and column 11 line 60 – column 12 line 4).

Referring to claim 3, Kurosaka further discloses a coverage measurement module which ascertains if node faults are detectable for those nodes in a first category and wherein the coverage of measurement module ignores those nodes in a second category. Where the nodes are categorized in the correspondence rules by logic type (see Kurosaka, column 8 lines 14-15) and the correspondence rules can then be used to select which nodes can be tested (see Kurosaka, column 7 lines 41-44).

Referring to claim 4, Kurosaka further discloses a system further comprising a test pattern profiling module configured to convert an existing test pattern into a pattern profile as specified by a profile mode (see Kurosaka, column 7 lines 38-49).

Referring to claim 5, Kurosaka further discloses a system further comprising a pattern checking module configured to process the pattern profile to produce analysis results indicative of whether the test pattern complies with a specified rule (see Kurosaka, column 10 lines 15-20).

Referring to claim 6, Kurosaka teaches all features of the claimed invention except for a test generator which generates a set of test vectors that are then sent to a simulated design which models the operational characteristics of the circuit design.

McNamara further discloses a test generator which generates a set of test vectors that are then sent to a simulated design which models the operational characteristics of the circuit design (see McNamara, column 3 lines 40-43 and column 3 lines 47-50).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because generating a set of test vectors which are sent to a simulated design to model the operational characteristics of the circuit design would have allowed the skilled artisan to thoroughly test the simulated device design.

Referring to claim 8, Kurosaka teaches all the features of the claimed invention except for a simulated design which receives test vectors and generates output data.

McNamara further teaches a simulated design which receives test vectors (i.e. input signals) and generates output data (see McNamara, column 3 lines 43-47).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka et al. to further include the teachings of McNamara because using a simulated design to generate output data would have allowed the skilled artisan to test the specified modules more efficiently.

Referring to claim 9, Kurosaka further discloses a data file which stores a detailed representation of the circuit information (see Kurosaka, column7 lines 6-9).

Referring to claim 11, Kurosaka discloses a system for verifying device design that includes functional modules (see Kurosaka, Figure 1, i.e. logic circuit verification device 100), wherein the system comprises; a profile generation means (see Kurosaka, Figure 1, i.e. data input unit 101) for providing a pattern profile (see Kurosaka, Figure 1, i.e. intermediate format data file 106) that represents a test pattern, wherein the pattern profile includes an intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode (see Kurosaka, column 8 lines 34-41), a coverage measurement means (see Kurosaka, Figure 1, i.e. corresponding point detection section 102) for analyzing the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation means is further configured to process the analysis results to provide an improved pattern profile (see Kurosaka, column 9 lines 31-40), and a pattern generation means for converting the improved pattern profile into a test pattern (see Kurosaka, column 8 lines 42-50). Kurosaka does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara teaches a test pattern as a time sequence (see McNamara, column 4 lines 46-65) of input signal vectors (see McNamara, column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara, column 5 lines 49-54 and column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara, column 6 lines 8-19).

Referring to claim 12, Kurosaka further teaches a coverage measurement means which is configured to determine the coverage of the test pattern by ascertaining if node faults are detectable (see Kurosaka, column 11 line 60-64).

Referring to claim 13, Kurosaka further discloses a test pattern profiling means for converting an existing test pattern into a pattern profile (see Kurosaka, column 7 lines 38-49).

Referring to claim 14, Kurosaka teaches all the features of the claimed invention except that the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design.

McNamara further discloses that the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design (see McNamara, column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because running the test

pattern on a simulation which implements a portion of a device design would have allowed the skilled artisan to ensure a complete test of the design.

Referring to claim 16, Kurosaka teaches that the device design includes functional modules each having module input signals and module output signals, and wherein the profile includes an intelligible representation of a test pattern for one of the functional modules.

McNamara further teaches a simulated design which receives test vectors (i.e. input signals) and generates output data (see McNamara, column 3 lines 43-47), where a test generator generates test vectors based on a design description (see McNamara, column 4 lines 38-39) coded in a known design language (see McNamara, column 3 lines 22-24).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kurosaka to further include the teachings of McNamara because including an intelligible representation of a test pattern would have allowed the skilled artisan to generate a more understandable process of the device design.

Referring to claim 17, Kurosaka discloses a method for verifying a device design comprising the steps; analyzing a test pattern profile to determine coverage of a test pattern (see Kurosaka, column 10 lines 62-63), generating a second profile for an improved test pattern that provides better coverage (see Kurosaka, column 10 lines 63-67), converting the second profile into the improved test pattern (see Kurosaka, column

10 line 67 – column 11 line 1) and running the improved test pattern on a simulated device (see Kurosaka, column 11 lines 2-3). Kurosaka does not teach a test pattern as a time sequence of input signal vectors with an associated sequence of output signal vectors.

McNamara teaches a test pattern as a time sequence (see McNamara, column 4 lines 46-65) of input signal vectors (see McNamara, column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara, column 5 lines 49-54 and column 5 line 60 – column 6 line 7).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because using a test pattern with an associated output would have allowed the skilled artisan to verify if the system is working correctly and identify any system errors (see McNamara, column 6 lines 8-19).

Referring to claim 18, Kurosaka discloses a method where the test pattern profile includes an intelligible representation of aspects of the test pattern, and where the aspects are specified by the profile module (see Kurosaka, column 7 lines 38-41).

Referring to claim 19, Kurosaka discloses a method where one aspect specified by the profile mode is a subset of input signals that represent instructions (see Kurosaka, column 7 lines 49-53).

Referring to claim 20, Kurosaka teaches all the features of the claimed invention except that one aspect specified by the profile mode is a set of input signals for a functional sub-module of the device design.

McNamara discloses a circuit design which is coded in a known software language and sent to a test generator which generates a set of test vectors that are then sent to a simulated design, which includes software, and this software then models the operational characteristics of the circuit design (see McNamara, column 3 lines 40-43 and column 3 lines 47-50).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka to further include the teachings of McNamara because breaking the input signals down by sub-modules of device design would have allowed the skilled artisan to ensure specific and relevant inputs to aid in detecting specific faults in the circuit design.

Claims 7, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosaka et al. (U.S. Patent No. 5,949,691) (hereinafter Kurosaka), in view of McNamara et al. (U.S. Patent No. 6,141,630) (hereinafter McNamara) and further in view of Valind (U.S. Patent No. 5,684,808).

Referring to claim 7, Kurosaka and McNamara teach all the features of the claimed invention except for a device design which has a set of interesting input signals and a set of customary input signals, wherein the profile includes a human-intelligible representation of the set of interesting input signals, and wherein the profile does not include any representation of the set of customary input signals.

Valind further discloses an automatic test pattern generator which is coupled to the detailed description (i.e. profile) and uses this information to generate test patterns for testing an integrated circuit (see Valind, column 8 lines 1-5), and a test generation function which automatically generates a test pattern to test for a determined fault (see Valind, column 11 lines 47-54).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka and McNamara to further include the teachings of Valind because generating a test pattern to test for a determined fault would have allowed the skilled artisan to efficiently test all aspects of the circuit design.

Referring to claim 10, Kurosaka and McNamara disclose all the features of the claimed invention except for a profile generation module which is configurable to generate sequential permutations of values to specify pattern profiles.

Valind teaches test patterns which are generated using an automatic test pattern generator and then fault simulated to determine the faults detected by the given pattern (see Valind, column 10 lines 30-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurosaka and McNamara to further include the teachings of Valind because generating sequential permutations of values to specify pattern profiles would have allowed the skilled artisan to ensure that all possible or relevant fault scenarios are covered.

Referring to claim 15, Kurosaka and McNamara teach all the features of the claimed invention except for a device design which has a first set of input signals and a second distinct set of input signals, wherein the profile includes an intelligible representation of the first set of input signals and wherein the profile does not include any representation of the second set of input signals.

Valind further discloses an automatic test pattern generator which is coupled to the detailed description (i.e. profile) and uses this information to generate test patterns for testing an integrated circuit (see Valind, column 8 lines 1-5), and a test generation function which automatically generates a test pattern to test for a determined fault (see Valind, column 11 lines 47-54).

It would have been obvious to one having ordinary skill in the art to modify Kurosaka and McNamara to further include the teachings of Valind because having a device design with two sets of input signals, one which is represented and one which is not would have allowed the skilled artisan to modify the device design input to match the design needs.

Response to Argument

11. Appellant argues that none of the applied references teach "a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors." However, while neither Kurosaka nor Valind are used to reject this limitation, it is considered met by McNamara et al. In McNamara et al., the design is tested with input values (i.e. input signal vectors) to determine stability (see McNamara

et al., column 5 lines 10-14). The output is compared with expected results (i.e. output signal vectors) and it is determined if the output is correct or incorrect (see McNamara et al., column 5 lines 15-31, and column 5 line 60 – column 6 line 7). Test vectors are created by the test generator and "generate input signals" by setting variables (see McNamara et al., column 6 lines 40-44) so that all paths can be tested and an output can be generated and compared to the expected values (see McNamara et al., column 6 lines 1-7). McNamara further discloses a test generator which correlates the test vectors (i.e. input) with the results from the function model (i.e. output) (see McNamara, column 5 lines 49-54). Correlating the input and output is used to determine which path within the design is operating incorrectly (see McNamara, column 5 lines 49-54). Therefore the Examiner concludes that McNamara et al. does teach a pattern profile that represents a sequence of input signal vectors (see McNamara, column 4 line 66 – column 5 line 4) with an associated sequence of output signal vectors (see McNamara, column 5 lines 49-54).

Appellant further argues that there is no motivation to combine Kurosaka and McNamara et al. (hereinafter McNamara); however, this is not the case. Kurosaka teaches an intermediate data file. This data file contains information pertaining to breakdown of the circuit for testing (see Kurosaka, column 8 lines 34-40). McNamara teaches a test generator for creating test vectors which contain both circuit path, or breakdown, data (see McNamara, column 4 lines 46-57) as well as input values (i.e. input signal vectors) to determine stability (see McNamara et al., column 5 lines 10-14); comparing the output with expected results (i.e. output signal vectors) and it is

determined if the output is correct or incorrect (see McNamara et al., column 5 lines 15-31, and column 5 line 60 – column 6 line 7). It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Kurosaka to include the teachings of McNamara because using a test pattern, which combines circuit design and timing data, with an associated output would have allowed the skilled artisan to localize and identify whether the design is operating correctly or incorrectly (see McNamara, column 6 lines 8-19).

Conclusion

12. For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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MKB
November 25, 2003

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